AMENDMENTS TO THE CLAIMS

Claim 1 (Original): A channel CODEC processor, comprising:

an algorithm-specific kernel block operable to receive a data stream, the kernel block comprising logic tailored to perform at least one step of a channel CODEC algorithm on the data stream; and

a processor core coupled to provide configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

Claim 2 (Original): The channel CODEC processor of claim 1, further comprising an interconnect through which data flows between the processor core and the algorithm-specific kernel block, wherein the processor core is operable to provide configuration data to the interconnect to control data-flow between the processor core and the algorithm-specific kernel block.

Claim 3 (Original): The channel CODEC processor of claim 1, wherein the configuration data controls operation parameters of the algorithm-specific kernel block.

Claim 4 (Original): The channel CODEC processor of claim 1, wherein the processor core is operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks.

Claim 5 (Original): The channel CODEC processor of claim 1, wherein the processor core is operable to perform another step of the channel CODEC algorithm.

Claim 6 (Original): The channel CODEC processor of claim 1, wherein the processor core is operable to perform steps of another channel CODEC algorithm.

Claim 7 (Original): The channel CODEC processor of claim 1, further comprising a local memory coupled to the processor core.

Claim 8 (Original): The channel CODEC processor of claim 1, further comprising a local memory coupled to the algorithm-specific kernel block.

Claim 9 (Original): The channel CODEC processor of claim 1, wherein the logic of the algorithm-specific kernel block is tailored to decode data in the data stream according to a Viterbi decoding algorithm.

Claim 10 (Original): The channel CODEC processor of claim 1, wherein the logic of the algorithm-specific kernel block is tailored to decode data in the data stream according to a convolutional decoding algorithm.

Claim 11 (Original): The channel CODEC processor of claim 1, wherein the logic of the algorithm-specific kernel block is tailored to decode data in the data stream according to a Turbo decoding algorithm.

Claim 12 (Original): The channel CODEC processor of claim 1, wherein the algorithm-specific kernel block comprises a reconfigurable encoder for convolutional codes in which at least one polynomial parameter of the encoder is controlled by the configuration data.

Claim 13 (Original): The channel CODEC processor of claim 1, wherein the algorithm-specific kernel block comprises a reconfigurable encoder for Turbo codes in which at least one polynomial parameter of the encoder is controlled by the configuration data.

Claim 14 (Original): The channel CODEC processor of claim 1, wherein the algorithm-specific kernel block comprises a reconfigurable cyclic-redundancy check (CRC) encoder.

Claim 15 (Original): The channel CODEC processor of claim 1, wherein the algorithm-specific kernel block comprises a reconfigurable cyclic-redundancy check (CRC) checker.

Claim 16 (Original): A channel CODEC processor, comprising:

a first algorithm-specific kernel block operable to receive a data stream, the first algorithm-specific kernel block comprising logic tailored to perform a step of a first channel CODEC algorithm on the data stream to generate a first processed data stream;

a second algorithm-specific kernel block coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step of a second channel CODEC algorithm on the first processed data stream to generate a second processed data stream; and

a processor core coupled to provide configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel CODEC algorithm and the step of the second channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

Claim 17 (Original): channel CODEC processor of claim 16, further comprising an interconnect through which data flows among the processor core and the algorithm-specific kernel blocks, wherein the processor core is operable to provide configuration data to the interconnect to control data-flow among the processor core and the algorithm-specific kernel blocks.

Claim 18 (Original): The channel CODEC processor of claim 16, wherein the first configuration data controls operation parameters of the first algorithm-specific kernel

block and wherein the second configuration data controls operation parameters of the second algorithm-specific kernel block.

Claim 19 (Original): The channel CODEC processor of claim 16, wherein the processor core is operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks.

Claim 20 (Original): The channel CODEC processor of claim 16, wherein the processor core is operable to perform steps of the first channel CODEC algorithm and the second channel CODEC algorithm.

Claim 21 (Original): The channel CODEC processor of claim 16, wherein the processor core is operable to perform steps of a third channel CODEC algorithm.

Claim 22 (Original): A channel CODEC processor, comprising:

an input operable to receive a data stream;

a plurality of processor cores including a first processor core and a second processor core operable to process data in the data stream;

a plurality of algorithm-specific kernel blocks including a first algorithm-specific kernel block and a second algorithm-specific kernel block coupled to the first processor core and the second processor core, respectively, wherein the first algorithm-specific

kernel block is operable to receive first data from the first processor core and to perform at least one step of a first channel CODEC algorithm on the first data, wherein the second algorithm-specific kernel block is operable to receive second data from the second processor core and to perform at least one step of a second channel CODEC algorithm on the second data.

Claim 23 (Original): The channel CODEC processor of claim 22 wherein operation parameters of the first algorithm-specific kernel block and the second algorithm-specific kernel block are user-configurable.

Claim 24 (Original): The channel CODEC processor of claim 22 wherein at least one of the processor cores is coupled to provide configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel CODEC algorithm and the step of the second channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

Claim 25 (Original): The channel CODEC processor of claim 22, further comprising an interconnect through which data flows among the processor cores and the algorithm-specific kernel blocks, wherein at least one of the processor cores is operable to provide configuration data to the interconnect to control data-flow between the processor cores and the algorithm-specific kernel blocks.

Claim 26 (Original): The channel CODEC processor of claim 22, wherein the processor cores are operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks.

Claim 27 (Original): The channel CODEC processor of claim 22, further comprising memories coupled to the processor cores.

Claim 28 (Original): The channel CODEC processor of claim 22, further comprising memories coupled to the algorithm-specific kernel blocks.

Claim 29 (Original): A communication device, comprising:

an I/O interface operable to couple to an antenna;

a modem device for modulating and demodulating data coupled to the I/O interface; and

a channel CODEC processor coupled to the modem device to receive a demodulated data stream, the channel CODEC processor comprising:

a first algorithm-specific kernel block operable to receive the demodulated data stream, the kernel block comprising logic tailored to perform at least one step of a channel decoding algorithm on the demodulated data stream; and

a first processor core coupled to provide first configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to

perform the at least one step of the channel decoding algorithm according to one of a plurality of wireless communication standards as specified by the first configuration data.

Claim 30 (Original): The channel CODEC processor of claim 29, wherein the first processor core is operable to perform steps of the channel decoding algorithm.

Claim 31 (Original): The communication device of claim 29, further comprising a network interface operable to receive a data stream from a network, and wherein the channel CODEC processor further comprises:

a second algorithm-specific kernel block operable to receive the data stream, the kernel block comprising logic tailored to perform at least one step of a channel encoding algorithm on the data stream;

a second processor core coupled to provide second configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel encoding algorithm according to one of a plurality of wireless communication standards as specified by the second configuration data.

Claim 32 (Original): The communication device of claim 31, wherein the second processor core is operable to perform steps of the channel decoding algorithm.

Claim 33 (Original): A communication device, comprising:

an I/O interface operable to couple to an antenna;

a modem device for modulating and demodulating data coupled to the I/O interface; and

a channel CODEC processor coupled to the modem device to receive a demodulated data stream, the channel CODEC processor comprising:

a first algorithm-specific kernel block operable to receive the demodulated data stream, the first algorithm-specific kernel block comprising logic tailored to perform a step of a first channel decoding algorithm on the demodulated data stream to generate a first processed data stream;

a second algorithm-specific kernel block coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step of a second channel decoding algorithm on the first processed data stream to generate a second processed data stream; and

a first processor core coupled to provide first configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel decoding algorithm and the step of the second channel decoding algorithm according to one of a plurality of wireless communication standards as specified by the first configuration data.

Claim 34 (Original): The communication device of claim 33, wherein the first processor core is operable to perform steps of the channel decoding algorithms.

Claim 35 (Original): The communication device of claim 33, further comprising a network interface operable to receive a data stream from a network.

Claim 36 (Previously Presented): The communication device of claim 35, wherein the channel CODEC processor further comprises:

a third algorithm-specific kernel block operable to receive the data stream from the network interface, the third algorithm-specific kernel block comprising logic tailored to perform a step of a first channel encoding algorithm on the data stream to generate a third processed data stream;

a fourth algorithm-specific kernel block coupled to the third algorithm-specific kernel block to receive the third processed data stream, the fourth algorithm-specific kernel block comprising logic tailored to perform a step of a second channel encoding algorithm on the first processed data stream to generate a fourth processed data stream; and

a second processor core coupled to provide second configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel encoding algorithm and the step of the second channel encoding algorithm according to one of a plurality of wireless communication standards as specified by the second configuration data.

Claim 37 (Original): The communication device of claim 36, wherein the second processor core is operable to perform steps of the channel encoding algorithms.